# Overview

This documentation is written for programmers, who wish to write software for the *MMC Replay*. The main focus in this document here is the description and explanation of all hardware registers and features.

The *MMC Replay* card is a design combination of the famous *Retro Replay* & *MMC64* C64 hardware products from Individual Computers into one single cartridge. It is 99% compatible with existing software written for both products, and its behaviour is modeled as if a *Retro Replay* card is plugged into the expansion connector of a MMC64 card. However, this hardware introduces several additional features, which greatly enhance the usefulness of both products this hardware represents.

***MMC Replay Hardware Specs***

- **512KB FLASH rom**
- **512KB SRAM**
- **1KB Serial EEPROM**
- **SPI Interface**
- **Clockport**
- **Freezer functionality**



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## Register Map

This section contains a raw description of all *MMC Replay* Registers and their respective bits.

*MMC Replay* maps its registers into both I/O areas. Its split register combination resembles pairing the *MMC64* with the *Retro Replay* memory map. To implement the additional features of the *MMC Replay* some register bits have changed or have additional meanings compared to both products. *Retro Replay* based registers are represented in blue, *MMC64* in yellow.

**$DE00: Freezer Control Register (write)**

| Bit | Description | R/W |
|---|---|---|
| 0 | GAME line | w |
| 1 | EXROM line | w |
| 2 | 1 = disable freezer registers | w |
| 3 | bank address 13 | w |
| 4 | bank address 14 | w |
| 5 | 0 = ROM enable , 1 = RAM enable | w |
| 6 | 1 = exit freezer mode | w |
| 7 | bank address 15 | w |

**$DE01: Ext. Freezer Control Register (write)**

| Bit | Description | R/W |
|---|---|---|
| 0 | 0 = dis. clock port , 1 = en. clock port | w |
| 1 | 0 = dis. io ram banking , 1 = allow banking | w |
| 2 | 0 = en. freeze button , 1 = dis. freeze | w |
| 3 | bank address 13 (mirror $de00) | w |
| 4 | bank address 14 (mirror $de00) | w |
| 5 | 0 = enable MMC registers , 1 = disable **(1)** | w |
| 6 | 0 = ram/rom @ $dfxx , 1 = ram/rom @ $dexx | w |
| 7 | bank address 15 (mirror $de00) | w |

**(1) Can only be written when bit 6 of $DF12 is 1. Register becomes effective when bit 0 of $DF11 is 1.**

| $DE00/01: Freezer Control Register (read) | | |
|---|---|---|
| **Bit** | **Description** | **R/W** |
| **0** | 0 = Flash write protected , 1 = write enabled | R |
| **1** | 0 = dis. io ram banking , 1 = allow banking | R |
| **2** | 1 = freeze button pressed | R |
| **3** | bank address 13 | R |
| **4** | bank address 14 | R |
| **5** | ****** not used ****** | R |
| **6** | 0 = ram/rom @ $dfxx , 1 = ram/rom @ $dexx | R |
| **7** | bank address 15 | R |

| $DE02-$DE0F: Clock Port Memory Area | | |
|---|---|---|
| **Bit** | **Description** | **R/W** |
| **„7-0“** | Byte is transferred to Clock Port | R/W |

| $DF10: SPI Transfer register | | |
|---|---|---|
| **Bit** | **Description** | **R/W** |
| **„7-0“** | Byte transferred to/from MMC/SD card | R/W |

| $DF11: MMC Replay Control Register | | |
|---|---|---|
| **Bit** | **Description** | **R/W** |
| **0** | 0 = MMC Bios ena. , 1 = MMC Bios dis. **(2)** | R/W |
| **1** | 0 = card selected , 1 = card deselected **(3)** | R/W |
| **2** | 0 = 250khz transfer , 1 = 8mhz transfer | R/W |
| **3** | ****** not used ****** | |
| **4** | ****** not used ****** | |
| **5** | GAME / EXROM enable , RAM mapping **(4)** | R/W |
| **6** | 0 = SPI write trigger , 1 = SPI read trigger | R/W |
| **7** | ****** not used ****** | |

**(2) Enabling MMC Bios sets ROM banking to the last 64K bank.**
**(3) This bit also controls the green activity LED.**
**(4) When in 8k freezer mode, bit 5 enables GAME/EXROM control bits.**
**When in MMC64 bios / 16k mode, bit 5 controls RAM mapping.**

| $DF12: MMC Replay Status Register | | |
|---|---|---|
| **Bit** | **Description** | **R/W** |
| **0** | 1 = set ROM write protection **(5)** | W |
| | 0 = SPI ready, 1 = SPI busy | R |
| **1** | feedback of $DE00 bit 0 (GAME) | R |
| **2** | feedback of $DE00 bit 1 (EXROM) | R |
| **3** | 0 = card inserted, 1 = no card inserted | R |
| **4** | 0 = card write ena., 1 = card write dis. | R |
| **5** | EEPROM DATA line / DDR Register **(6)** | R/W |
| **6** | 0 = RR compatibility mode, 1 = Ext. mode **(7)** | R/W |
| **7** | EEPROM CLK line | W |

**(5) Setting this bit will disable writes to ROM until next reset.**
**(6) Setting DATA to "1" enables reading data bit from EEPROM at this position.**
**(7) Selecting RR compatibility mode limits RAM to 32K and disables writes to Extended Banking Register.**
**Selecting Extended mode enables full RAM banking and enables Nordic Power mode in 8k ROM mode.**

| $DF13: Extended Banking Register (8) | | |
|---|---|---|
| **Bit** | **Description** | **R/W** |
| **0** | bank address 16 | R/W |
| **1** | bank address 17 | R/W |
| **2** | bank address 18 | R/W |
| **3** | ****** not used ****** | |
| **4** | ****** not used ****** | |
| **5** | 0 = 8k ROM mapping , 1 = 16k ROM mapping | R/W |
| **6** | 1 = enable freezer registers | W |
| **7** | ****** not used ****** | |

**(8) Can only be read/written to when bit 6 of $DF12 is 1.**

# MMC Replay Memory Mapping

Due to the flexibility of the hardware, *MMC Replay* implements a complex memory mapping system which was developed with both backwards compatibility to *Retro Replay* and *MMC64* as well as further enhancements in mind.

One can distinguish between 3 basic memory schemes of the MMC Replay:

- **MMC Replay Bios Mode**
- **8KB Freezer Mode**
- **16KB Freezer Mode**

This manual will now discuss the basic memory layout of each Scheme, with the processor registers being $00 = $e2, $01 = $e7.

## MMC Replay Bios Mode

In MMC Replay Bios Mode, the ROM bank is normally fixed to bank 7 when RAM is disabled. When enabling RAM, one can select between 2 different RAM modes using bit#5 of $DF11. Note that RAM enabled at $8000 is read only while RAM mapped at $E000 is both read and write enabled. GAME & EXROM bits have no effect, the serial EEPROM can be accessed.

**Standard ROM map**

| C64 Memory Map | |
|---|---|
| **Address** | **Content** |
| $0000 | 8KB RAM |
| $2000 | 8KB RAM |
| $4000 | 8KB RAM |
| $6000 | 8KB RAM |
| $8000 | MMC REPLAY BIOS |
| $A000 | MMC REPLAY BIOS (MIRROR) |
| $C000 | RAM |
| $D000 | I/O |
| $E000 | KERNAL |

**RAM & $DF11 bit#5 = 1**

| C64 Memory Map | |
|---|---|
| **Address** | **Content** |
| $0000 | 8KB RAM |
| $2000 | 8KB RAM |
| $4000 | 8KB RAM |
| $6000 | 8KB RAM |
| $8000 | 512K RAM READ WINDOW |
| $A000 | MMC REPLAY BIOS (MIRROR) |
| $C000 | RAM |
| $D000 | I/O |
| $E000 | KERNAL |

**RAM & $DF11 bit#5 = 0**

| C64 Memory Map | |
|---|---|
| **Address** | **Content** |
| $0000 | 8KB RAM |
| $2000 | 8KB RAM |
| $4000 | 8KB RAM |
| $6000 | 8KB RAM |
| $8000 | MMC REPLAY BIOS |
| $A000 | MMC REPLAY BIOS (MIRROR) |
| $C000 | RAM |
| $D000 | I/O |
| $E000 | 512K RAM READ & WRITE WINDOW |

**MMC Replay Bios Register config:**

**$DF11: bit#0 = 0**

# 8KB Freezer Mode

8KB freezer mode is compatible with Action Replay, Retro Replay & Nordic Power ROMS. The memory configuration is controlled by setting the GAME & EXROM lines of the PLA using bit#0 & bit#1 of $DE00.

On the left, one can see the possible bit configurations of this mode. Note that bit#5 of $DE00 enables RAM at $8000, which is normally read only, except in Ultimax mode where the C64 PLA allows write accesses to this area. You can disable ROM/RAM mapping by setting GAME=0 & EXROM=1.

MMC Replay supports the special Nordic Power mode, which allows both ROM and RAM accesses.

When pressing Freeze, GAME & EXROM are disabled & the memory map changes to Freeze mode. Furthermore, banking bits 13-15 & the RAM enable bit are cleared. This mode can be left again by setting bit#6 of $DE00.

```
8KB Freezer Mode Register Config:
    $DF11: bit#0 = 1
           bit#5 = 0
    $DF13: bit#5 = 0
```

GAME=0 , EXROM=0

| C64 Memory Map | |
|---|---|
| Address | Content |
| $0000 | 8KB RAM |
| $2000 | 8KB RAM |
| $4000 | 8KB RAM |
| $6000 | 8KB RAM |
| $8000 | 8KB ROM BANK / 8KB RAM (R) |
| $A000 | BASIC ROM |
| $C000 | RAM |
| $D000 | I/O |
| $E000 | KERNAL |

GAME=1 ,EXROM=0

| C64 Memory Map | |
|---|---|
| Address | Content |
| $0000 | 8KB RAM |
| $2000 | 8KB RAM |
| $4000 | 8KB RAM |
| $6000 | 8KB RAM |
| $8000 | 8KB ROM BANK / 8KB RAM (R) |
| $A000 | 8KB ROM BANK (MIRROR) |
| $C000 | RAM |
| $D000 | I/O |
| $E000 | KERNAL |

Freeze Mode

| C64 Memory Map | |
|---|---|
| Address | Content |
| $0000 | 4KB RAM |
| $1000 | NOTHING |
| $2000 | NOTHING |
| $4000 | NOTHING |
| $6000 | NOTHING |
| $8000 | NOTHING |
| $A000 | NOTHING |
| $C000 | NOTHING |
| $D000 | I/O |
| $E000 | 8KB ROM BANK |

GAME=1 , EXROM=1 (Ultimax Mode)

| C64 Memory Map | |
|---|---|
| Address | Content |
| $0000 | 4KB RAM |
| $1000 | NOTHING |
| $2000 | NOTHING |
| $4000 | NOTHING |
| $6000 | NOTHING |
| $8000 | 8KB ROM BANK /8KB RAM (R/W) |
| $A000 | NOTHING |
| $C000 | NOTHING |
| $D000 | I/O |
| $E000 | 8KB ROM BANK |

GAME=0, EXROM=1 , RAM=1, $DF12 bit#4=1 (Nordic Power Mode)

| C64 Memory Map | |
|---|---|
| Address | Content |
| $0000 | 8KB RAM |
| $2000 | 8KB RAM |
| $4000 | 8KB RAM |
| $6000 | 8KB RAM |
| $8000 | 8KB ROM BANK / 8KB RAM (R) |
| $A000 | 8KB RAM BANK (R/W) |
| $C000 | RAM |
| $D000 | I/O |
| $E000 | KERNAL |

# 16KB Freezer Mode

16KB freezer mode has been designed to provide additional functionality to the MMC Replay. The main difference between the 8K mode are that 2 * 8K banks are now supported & the freeze mode is much more flexible now.

**GAME=0 , EXROM=0**

| C64 Memory Map | |
|---|---|
| Address | Content |
| $0000 | 8KB RAM |
| $2000 | 8KB RAM |
| $4000 | 8KB RAM |
| $6000 | 8KB RAM |
| $8000 | 8KB ROM/RAM BANK LO(A13=0) |
| $A000 | BASIC ROM |
| $C000 | RAM |
| $D000 | I/O |
| $E000 | KERNAL |

**GAME=1 ,EXROM=0**

| C64 Memory Map | |
|---|---|
| Address | Content |
| $0000 | 8KB RAM |
| $2000 | 8KB RAM |
| $4000 | 8KB RAM |
| $6000 | 8KB RAM |
| $8000 | 8KB ROM/RAM BANK LO(A13=0) |
| $A000 | 8KB ROM/RAM BANK HI(A13=1) |
| $C000 | RAM |
| $D000 | I/O |
| $E000 | KERNAL |

**GAME=1 , EXROM=1 (Ultimax)**

| C64 Memory Map | |
|---|---|
| Address | Content |
| $0000 | 4KB RAM |
| $1000 | NOTHING |
| $2000 | NOTHING |
| $4000 | NOTHING |
| $6000 | NOTHING |
| $8000 | 8KB ROM/RAM BANK LO(A13=0) |
| $A000 | NOTHING |
| $C000 | NOTHING |
| $D000 | I/O |
| $E000 | 8KB ROM/RAM BANK HI(A13=1) |

**16KB Freezer Mode Register Config:**

**$DF11: bit#0 = 1**
**$DF13: bit#5 = 1**

**$DE00 bit#5=1**
**$DF11 bit#5=0**

| C64 Memory Map | |
|---|---|
| Address | Content |
| $0000 | 8KB RAM |
| $2000 | 8KB RAM |
| $4000 | 8KB RAM |
| $6000 | 8KB RAM |
| $8000 | 8KB RAM BANK LO(A13=0) |
| $A000 | 8KB ROM BANK HI(A13=1) |
| $C000 | RAM |
| $D000 | I/O |
| $E000 | KERNAL |

**$DE00 bit#5=1**
**$DF11 bit#5=1**

| C64 Memory Map | |
|---|---|
| Address | Content |
| $0000 | 8KB RAM |
| $2000 | 8KB RAM |
| $4000 | 8KB RAM |
| $6000 | 8KB RAM |
| $8000 | 8KB RAM BANK LO(A13=0) |
| $A000 | 8KB RAM BANK HI(A13=1) |
| $C000 | RAM |
| $D000 | I/O |
| $E000 | KERNAL |

Note that you can choose between 16KB ROM, 8KB RAM/8KB ROM and 16KB RAM configurations by setting the right bit#5 combination in both $DE00 and $DF11.

As with the 8KB Freezer Mode, you can disable ROM/RAM mapping by setting GAME = 0 & EXROM = 1.

Note that bank A13 register bit has no effect anymore, since it is now directly connected to CPU A13.

# 16KB Freezer Mode – Freeze memory map

As already mentioned, setting 16KB freezer mode changes the behaviour of the memory map after freeze has been pressed. RAM at $8000 is enabled by default and additionally, you can actually freeze from code placed in the 512K SRAM by setting $DF11 bit#5=1 before freezing, since this bit is NOT cleared during freeze.

As with the 8KB Freezer Mode, banking bits 13-15 & the RAM enable bit are cleared during freeze. You can also leave the freeze mode by setting bit#6 of $DE00.

**Freeze Mode $DF11 bit #5 = 0**

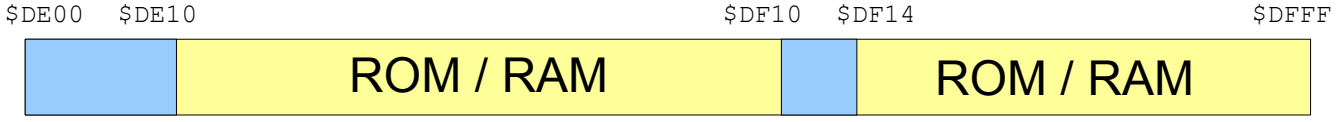
| C64 Memory Map | |
|---|---|
| **Address** | **Content** |
| $0000 | 4KB RAM |
| $1000 | NOTHING |
| $2000 | NOTHING |
| $4000 | NOTHING |
| $6000 | NOTHING |
| $8000 | 8KB RAM BANK LO(A13=0) |
| $A000 | NOTHING |
| $C000 | NOTHING |
| $D000 | I/O |
| $E000 | 8KB ROM BANK HI(A13=1) |

**Freeze Mode $DF11 bit #5 = 1**

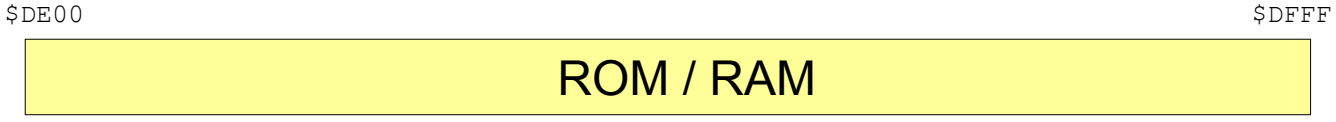
| C64 Memory Map | |
|---|---|
| **Address** | **Content** |
| $0000 | 4KB RAM |
| $1000 | NOTHING |
| $2000 | NOTHING |
| $4000 | NOTHING |
| $6000 | NOTHING |
| $8000 | 8KB RAM BANK LO(A13=0) |
| $A000 | NOTHING |
| $C000 | NOTHING |
| $D000 | I/O |
| $E000 | 8KB RAM BANK HI(A13=1) |

## I/O Memory Mapping

In addition to the standard memory mapping, MMC Replay also supports mapping of RAM or ROM into the IO area. In general, when mapping is enabled, memory surrounds the register locations occupied by MMC Replay.

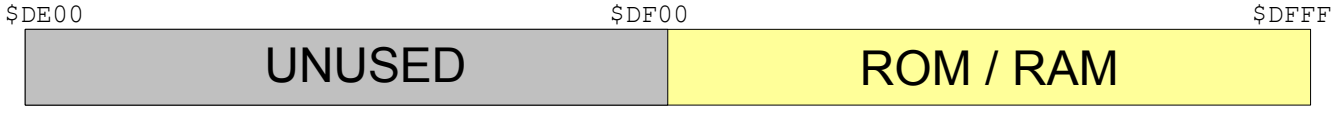



By deactivating those registers, you can access the full 512 byte memory.

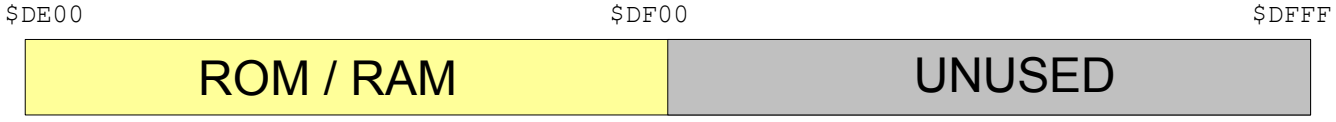



Since MMC Replay is backwards compatible with Retro Replay, the I/O area is split in 2 * 256 byte areas where memory can be mapped. However, in Bios Mode and 16KB Freezer Mode, you have both areas for 512 byte memory.

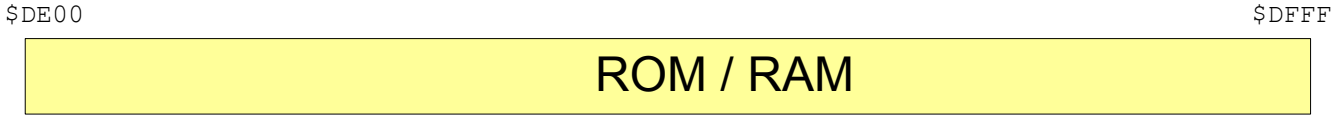
**8 KB Freezer Mode , Bios Mode , $DE01 bit#6 = 0**




**8 KB Freezer Mode , $DE01 bit#6 = 1**




**16 KB Freezer Mode , Bios Mode $DE01 bit#6 = 1**




To add Action Replay compatibility, which has only 8KB of RAM, an additional bit was introduced in the Retro Replay to allow banking in the I/O area. Setting bit#1 of $DE01 allows all banking bits to be enabled in the I/O area, disabling this bit disables banking bits 13-15 in this area. When in MMC Replay Bios mode, disabling this bit additionally disables banking bits 18-16 in the I/O area.

$DE00 - $DFFF is a mirror of $9E00-$9FFF.

# Last words of advice

- Please do not modify the contents of the serial EEPROM. Most users will not appreciate the change of configuration data. Furthermore, the data structures in the EEPROM will change in the future.

- The Serial EEPROM is only accessible in MMC Replay Bios mode.

- The MMC-Replay Bios sets the following configurations:

  ACTION REPLAY: allowbank = 0, $DF10-$DF13 registers disabled. Nordic Power enabled.
  RETRO REPLAY: $DE01 unset, $DF10-$DF13 registers disabled.
  SUPER MAPPER: $DE01 unset, 16K mode, $DF10-$DF13 registers enabled.
  RR + MMC64: $DE01 unset, $DE10-$DE13 registers enabled.

- Disabling Freezer registers also disables ALL ROM/RAM banking.

- When writing software for both MMC64 and MMC Replay, please consider the different MMC register disabling procedures between the 2 cartridges.

**This documentation is still PRELIMINARY & is going to be changed in the future.**



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